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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/662,233

09/15/2003

Joseph Kover JR.

9431

7590

02/25/2005

Joseph Kover, Jr.
974 North Aspen Way
Layton, UT 84040

EXAMINER

KITOV, ZEEV

ART UNIT

PAPER NUMBER

2836

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/662,233

Applicant(s)

KOVER ET AL.

Examiner

Zeev Kitov

Art Unit

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Objection

Claim 6 is objected to due to a following phrase: "high input control current" and "high input control current device", which do not make sense. For purpose of examination the phrases were interpreted as follows: "high current control input" and "high current input control device".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is a following phrase: "wherein the time interval between when the digital sequence either increments or decrements can be of one value for $t = 0$ to $t = 1$, a second value at $t = 1$ to $t = 2$, and a third value at $t = 2$ to $t = 3$ ". It is not clear, how the time interval can has different values at different times". The sentence does not make a sense. For purpose of examination it was interpreted as follows: "wherein the values of the digital sequence either increments or decrements can be of one value for $t = 0$ to $t = 1$, a second value at $t = 1$ to $t = 2$, and a third value at $t = 2$ to $t = 3$ ".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Tsuchida et al. (US 6,545,513). Tsuchida et al. disclose all the elements of Claim 1 including a system to dynamically control the rate of change of the DC current through a load circuit and/or the DC voltage across a load circuit, with respect to time, during the initial power up phase and during successive power up, power down, and power up cycles including: an equivalent digital sequencing means (element 104 in Fig. 7 and 8) initiating a digital sequence and whereby the digital sequence either increments or decrements, as required, at a given time interval (shown in Fig. 9), an equivalent drive circuit means (element 103 in Fig. 7 and 8) converting the digital sequence to an analog voltage level; an equivalent current control means (elements 105 and 113 in Fig. 7) controlling the current through a load circuit. The digital sequence inherently consists of either increments or decrements, as is evident from Fig. 8, wherein a capacitor (element 134 in Fig. 8) is an element accumulating (integrating) the increments/decrements.

Regarding Claim 2, Tsuchida et al. disclose an equivalent means to store the digital sequence and the time interval that the digital sequence either increments or decrement. Digital sequencing means (element 104 in Fig. 7 and 8) inherently has a memory storing the digital sequence. As taught in the College Digital Design Courses,

generation of the time sequence requires a sequential circuit, which by definition has memory (storage) elements. An appropriate reference will be provided upon request.

It further disclose the values of the digital sequence either increments or decrements can be of one value for $t = 0$ to $t = 1$, a second value at $t = 1$ to $t = 2$, and a third value at $t = 2$ to $t = 3$ (shown in Fig. 9).

Regarding Claim 3, Tsuchida et al. disclose further comprising an equivalent current measurement means (elements 105 in Fig. 7) and/or a voltage measurement means and whereby the current measurement means and/or the voltage measurement means activates a fault indication means (elements 113 in Fig. 7) if the current level and/or the voltage level is either greater than or less than the programmed current and/or the programmed voltage level.

Regarding Claim 4, Tsuchida et al. disclose an equivalent switching means (element 11 in Fig. 1) isolating the DC power supply from the load circuit whereby the switching means serves to delay the application of the DC current/voltage from the DC power supply to the load circuit (col. 27, lines 26 – 35) for the initialization of the system to dynamically control the rate of change of the DC current through a load circuit and/or the DC voltage across a load circuit, with respect to time.

Regarding Claim 5, Tsuchida et al. disclose an equivalent programming means to interactively establish the maximum DC current through a load circuit and/or the DC voltage across a load circuit (col. 14, lines 1 – 36).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillberg et al. (US 4,216,393) in view of Tsushida et al. and Sedra et al. Microelectronic Circuits. Gillberg et al. disclose an equivalent control means consisting of a MOS field effect transistor (element Q3 in Fig. 1), whereby the low output power device (element 14 in Fig. 1) connects to the gate of the transistor and whereby the transistor serves as a high input impedance buffer between the low output power device and the device (element Q1 in Fig. 1), which requires a high input control current, an equivalent means for the input current control of the high current input control device is provided by means of the drain source channel of the MOS field effect transistor (element Q3 in Fig. 1) to the base of the high current control device (element Q1 in Fig. 1). It further discloses a high input control current power device as a bipolar junction transistor (element Q1 in Fig. 1), whereby the base of said transistor is connected to the drain of the metal oxide semiconductor field effect transistor. However, it does not disclose the resistor connected between a power supply source and the drain of the MOS transistor. Tsushida et al. disclose an equivalent current/voltage bias control means consisting of a resistor (element R112 in Fig. 15) located between a positive DC current/voltage source

and the drain of the metal oxide semiconductor field effect transistor (element Q112 in Fig. 15). Both references have the same problem solving area, namely providing controlled load current rise and fall times. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Gillberg et al. solution by adding the resistor according to Tsushida et al., because as Tsushida et al. state (col. 23, line 56 – col. 24, line 12), the resistor detects a load current value and cooperatively function with transistor (element Q112 in Fig. 15) as a current drive section of the circuit. In the Gillberg et al. circuit modified according to Tsushida et al., the resistor is being located between a DC voltage source and the drain of the metal oxide semiconductor field effect transistor. Additionally, Gillberg et al. disclose the bipolar junction transistor as being connected by its collector to the power supply source and by its emitter to the load, i.e. in reversed way with respect to the Claim 6. Sedra et al. textbook discloses both MOS field effect transistors exist in two polarity different versions, having N and P channels (NMOS and PMOS) with similar characteristics but having opposite (with respect to a power source polarity) connections (see pages 344 – 345, Fig. 7.17). As is seen from Fig. 7.17, the N and P channel MOS transistors are mutually replaceable with change of polarity of both input and output signals. Sedra et al. textbook further discloses that the bipolar junction transistors exist in two polarity different versions NPN and PNP, with similar characteristics but having opposite (with respect to a power source polarity) connections (see page 409, Fig. 8.10). As is seen from Fig. 8.10, the NPN and PNP bipolar junction transistors are mutually replaceable with change of polarity of both input and output signals. Therefore,

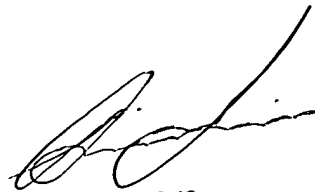
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the circuit consisting of P channel MOSFET and NPN transistor (shown in Fig. 1 of Gillberg) can be modified according to teaching of Sedra et al. thus producing a circuit consisting of N channel MOSFET and PNP transistor. The obtained circuit will have the same characteristics as the one shown in Fig. 1 of Gillberg, with only exception of signals polarity. In such modified circuit the bipolar PNP transistor is connected by its emitter to the power supply source and by its collector to the load.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
02/09/2005



BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800